FM4442
256 Bytes Memory Card Chip

Datasheet

Dec. 2008

Product Overview

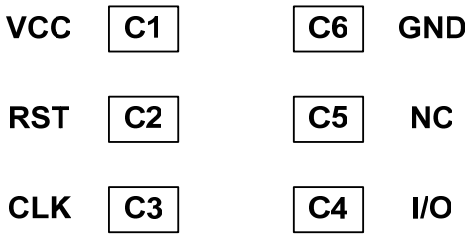
Description

FM4442 is the memory card chip developed by Shanghai FM Co., Ltd. This chip has 256×8 Bits EEPROM with write protect function and programmable security code. With its contact configuration in accordance to ISO standard 7816 (synchronous transmission), FM4442 can be widely used in different types of IC memory cards.

Features

- 256×8-bits EEPROM organization；
- Byte-wise addressing
- 32×1-bit organization of protection memory
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 0 ... 31)
- Two-wire link protocol
- End of processing indicated at data output
- Answer-to-Reset acc. to ISO standard 7816-3
- Data retention for minimum of ten years
- Programming time 2.5 ms per byte for both erasing and writing
- Contact configuration and serial interface in accordance with ISO standard 7816 (Synchronous transmission)
- Data can only be changed after entry of the correct 3-byte programmable security code (security memory)
- Compatible SLE4442

Pin Assignment



Pin Function

Pin	Symbol	Function
C1	VCC	Supply voltage 2.5V ~ 5V
C2	RST	Reset
C3	CLK	Clock input
C4	I/O	Bidirectional data line (open drain)
C5	NC	Not Connected
C6	GND	Ground

Function Description

The FM4442 consists of 256 x 8 bits EEPROM main memory and a 32-bit protection memory with PROM functionality. The main memory is erased and written byte by byte. Each of the first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased (PROM).

Reset and Answer-to-Reset

Answer-to-Reset takes place according to ISO standard 7816-3 (ATR). The reset can be given at any time during operation. In the beginning, the address counter is set to zero together with a clock pulse and the first data bit (LSB) is output to I/O when RST is set from level H to level L. Under a continuous input of additional 31 clock pulses the contents of the first 4 EEPROM addresses is read out. The 33rd clock pulse switches I/O to high impedance Z and finishes the ATR procedure.

Answer-to-Reset	Byte1	Byte 2	Byte 3	Byte 4
(HEX)	$DO_7 \ldots DO_0$	$DO_{15} \ldots DO_8$	$DO_{23} \ldots DO_{16}$	$DO_{31} \ldots DO_{24}$

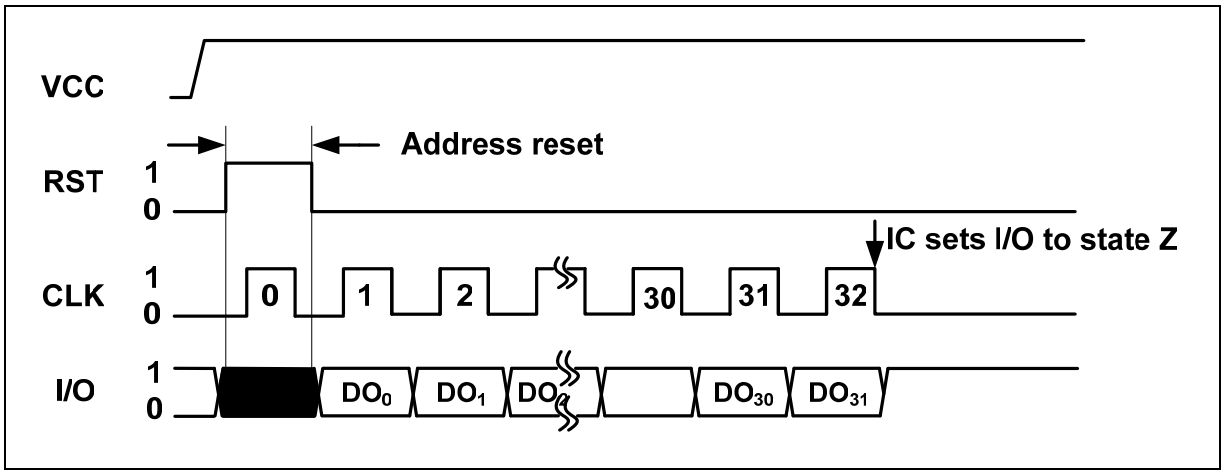


Figure 2 Reset and Answer-to-Reset

Commands

Commands Format：

MSB							LSB	MSB							LSB	MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Command Introduction

(1) Read Main Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	0	0	Address	No effect
Hexadecimal	30_H								00_H…FF_H	No effect

The command reads out the contents of the main memory (with LSB first) starting at the given byte address (N = 0…255) up to the end of the memory. After the command entry the IFD has to supply sufficient clock pulses. The number of clocks is m = (256 - N) × 8 + 1. The read access to the main memory is always possible.

(2) Read Protection Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	1	0	0	No effect	No effect
Hexadecimal	34_H								No effect	No effect

The command transfers the protection bits under a continuous input of 32 clock pulses to the output. I/O is switched to high impedance Z by an additional pulse. The protection memory can always be read, and indicates the data bytes of the main memory protected against changing.

(3) Update Main Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	0	0	0	Address	Input data
Hexadecimal	38_H								00_H…FF_H	Input data

The command programs the addressed EEPROM byte with the data byte transmitted. Depending on the old and new data, one of the following sequences will take place during the processing mode:
- erase and write (5 ms) corresponding to m = 245 clock pulses
- write without erase (2.5 ms) corresponding to m = 124 clock pulses
- erase without write (2.5 ms) corresponding to m = 124 clock pulses

(All values at 50 kHz clock rate.)

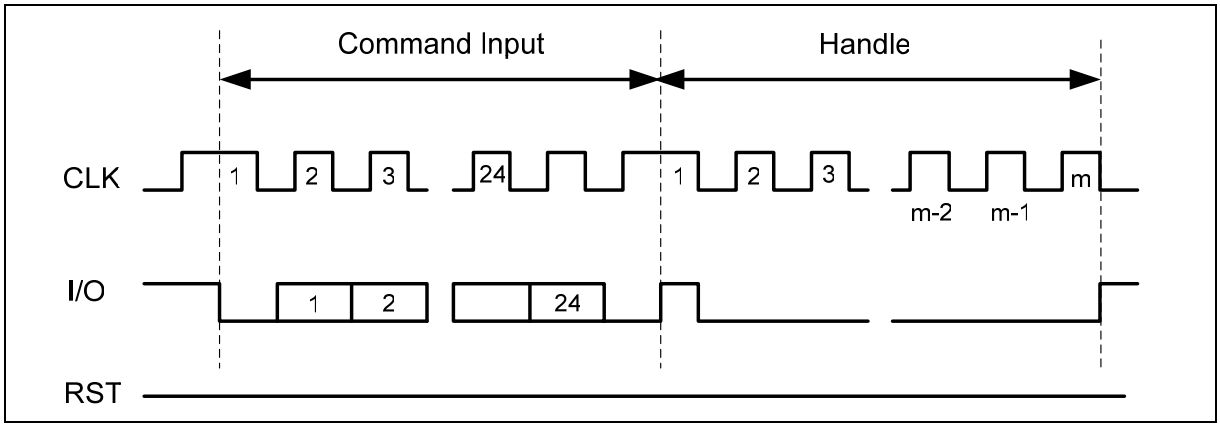


Figure 3 Update main memory

(4) Write Protection Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	1	0	0	Address	Input data
Hexadecimal	$3C_H$								00_H…$1F_H$	Input data

The execution of this command contains a comparison of the entered data byte with the assigned byte in the EEPROM. In case of identity the protection bit is written thus making the data information unchangeable. If the data comparison results in data differences writing of the protection bit will be suppressed.

(5) Read Security Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	0	1	No effect	No effect
Hexadecimal	31_H								No effect	No effect

Similar to the read command for the protection memory this command reads out the 4 bytes of the security memory.

(6) Update Security Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	0	0	1	Address	Input data
Hexadecimal	39_H								00_H…$1F_H$	Input data

Regarding the reference data bytes this command will only be executed if a PSC has been successfully verified before. Otherwise only each bit of the error counter (Address 0) can be written from “1” to “0”. The execution times and the required clock pulses are the same as described under update main memory.

(7) Compare Verification Data

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	1	1	Address	Input data
Hexadecimal	33_H								00_H…03_H	Input data

The command compares one byte of the entered verification data byte with the corresponding reference data byte.

PSC Verification

The FM4442 requires a correct verification of the Programmable Security Code PSC stored in the Security Memory for altering data if desired. The following table gives an overview of the necessary commands for the PSC verification. The sequence of the shaded commands is mandatory.

Command	Control	Address	Data	Remark
	B7…B0	A7…A0	D7…D0	
Read security memory	31_H	No effect	No effect	Check error counter
Update security memory	39_H	00_H	Input data	Write free bit in error counter input data: 0000 0ddd binary
Compare verification data	33_H	01_H	Input data	Reference data byte1
Compare verification data	33_H	02_H	Input data	Reference data byte2
Compare verification data	33_H	03_H	Input data	Reference data byte3
Update security memory	39_H	00_H	FF_H	Erase error counter
Read security memory	31_H	No effect	No effect	Check error counter

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-0.3	-	6	V
Input voltage	V_i	-0.3	-	6	V
Storage temperature	T_{sto}	-25	-	+70	℃
Power dissipation	P_{tot}	-	-	70	mW

Operation Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient temperature	T_A	-20	-	+60	℃
Supply Voltage	V_{CC}	2.5	5.0	5.5	V

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{cc}	-	3	10	mA
High level input voltage (I/O, CLK, RST)	V_{ih}	0.7 Vcc	-	Vcc	V
Low level input voltage (I/O, CLK, RST)	V_{il}	0	-	0.3* Vcc	V
High level input current (I/O, CLK, RST)	I_h	-	-	50	μA
Low level output current (V_{OL} = 0.4V, open drain)	I_{ol}	1	-	-	mA
High level output current (V_{OH} = 5V, open drain)	I_{oh}	-	-	50	μA
Input capacitance	C_i	-	-	10	pF

AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency f_{CLK}	f_{CLK}	7		50	kHz
I/O High time (Start Condition)	t_1	10			μs
CLK High to I/O Hold time	t_2	4			μs
I/O Low to CLK Hold time (Start Condition)	t_3	4			μs
I/O Setup to CLK High time	t_4	1			μs
CLK Low to I/O Hold time	t_5	1			μs
CLK High to I/O Clear time (Stop Condition)	t_6	4			μs
CLK Low to I/O Valid time	t_7			2.5	μs
CLK Low to I/O Valid time	t_8			2.5	μs
CLK Low to I/O Clear time	t_9			2.5	μs
RST High to CLK Setup time	t_{10}	4			μs
CLK Low to RST Hold time	t_{11}	4			μs
RST High time (address reset) time	t_{12}	20	50		μs
RST Low to I/O Valid time	t_{13}			2.5	μs
RST Low to CLK Setup time	t_{14}	4			μs

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK High time	t_{15}	9			µs
CLK Low time	t_{16}	9			µs
CLK Low to I/O Valid time	t_{17}			2.5	µs
Reset time for Break	t_{18}	5			µs
RST High to I/O Clear time (Break)	t_{19}	2.5			µs
CLK Rise time	t_R			1	µs
CLK Fall time	t_F			1	µs
Erase time	t_{ER}	2.5@ f_{CLK} = 50kHz			ms
Write time	t_{WR}	2.5@ f_{CLK} = 50kHz			ms
Power on reset time				100	µs

Timing Diagrams

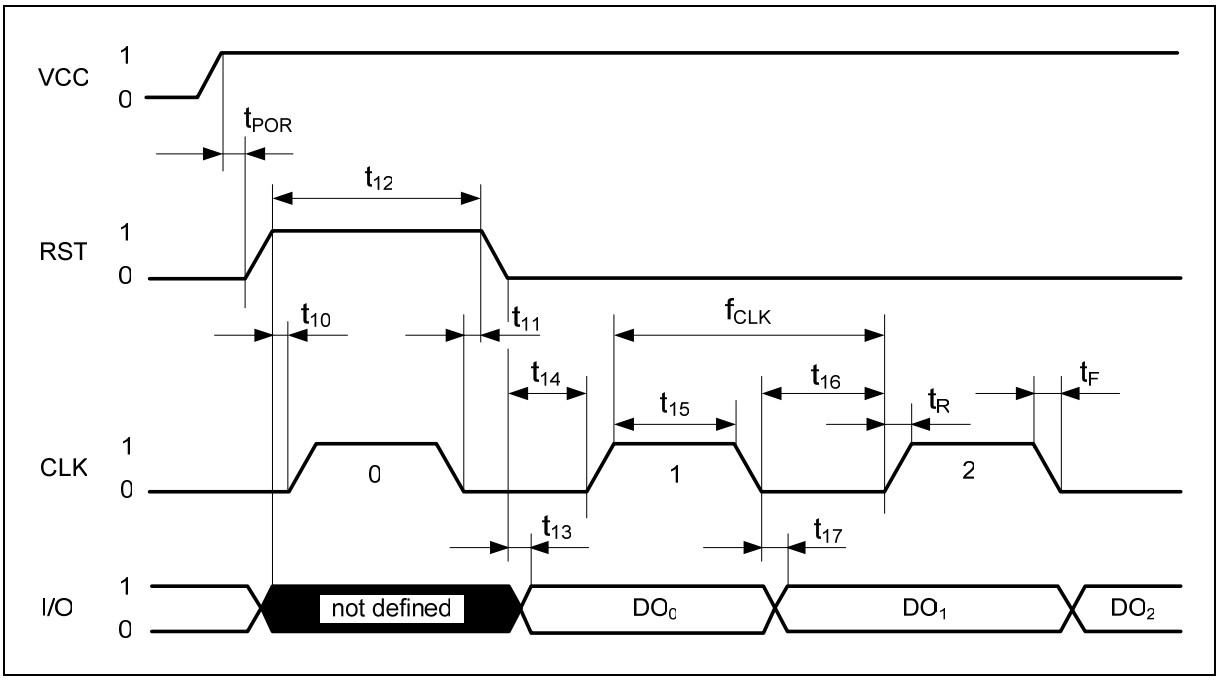


Figure 4 FM4442 Reset and Answer-to-Reset

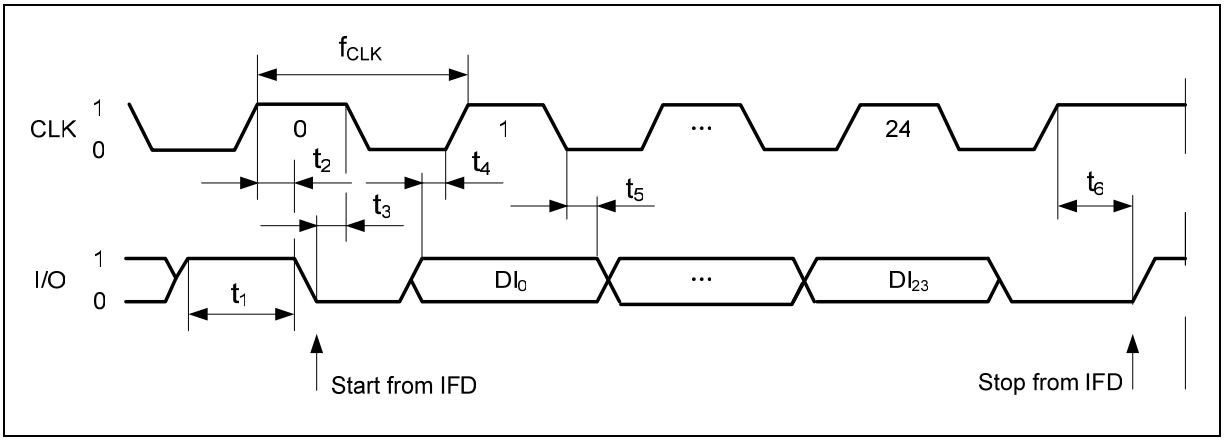


Figure 5 FM4442 Command Mode

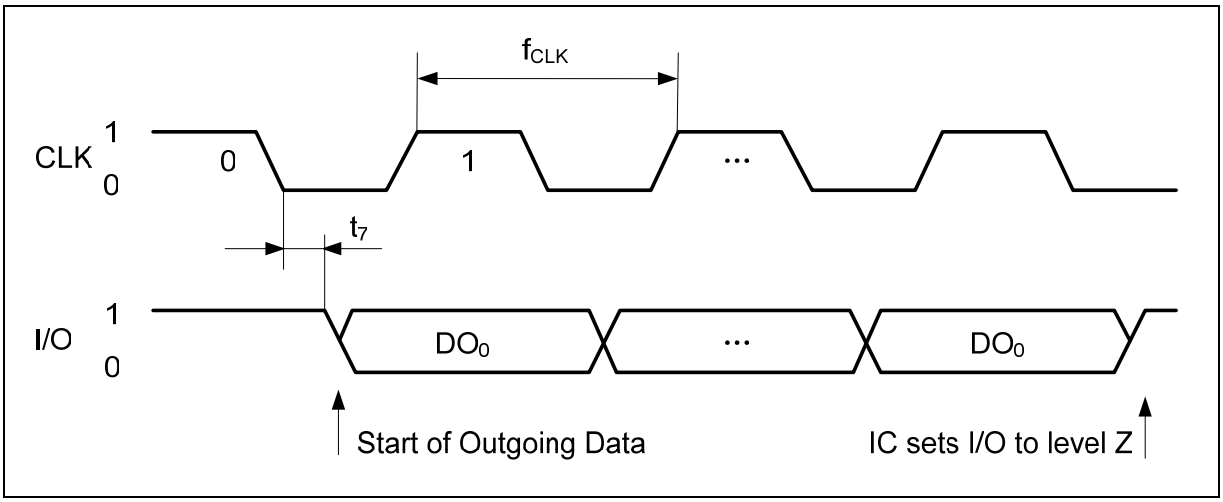


Figure 6 FM4442 Outgoing Data Mode

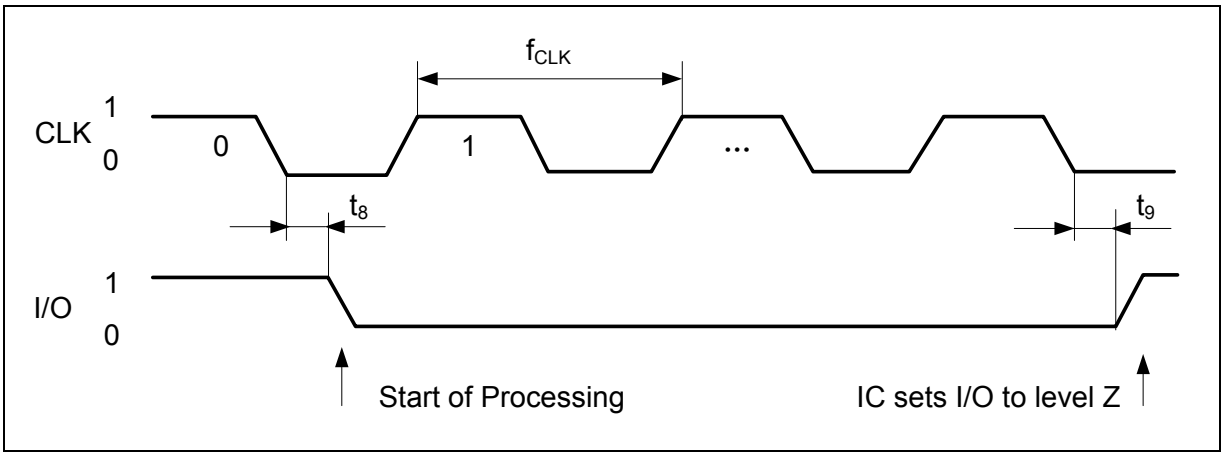


Figure 7 FM4442 Processing Mode

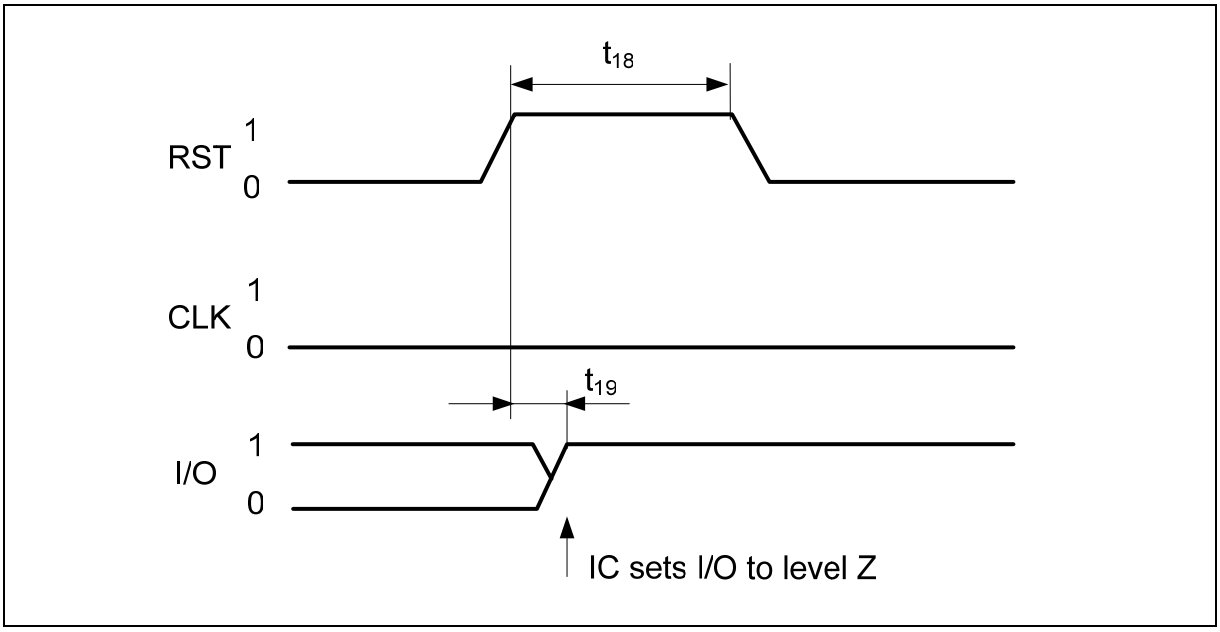


Figure 8 FM4442 Break